APM32F103xC

Errata Sheet

Version: V 2.1

Contents

1 Introduction

This Manual mainly introduces the limitations of the APM32F103xC series products during use. If you encounter the application scenarios described in the manual during the use of the product, please use the product according to the solutions provided in the manual; if no solution is provided, please avoid this application scenario.

2 Errata List

Table 1 Errata List

Category	Introduction	Product version	
		A1	A2
GPIO	GPIO output	●	●
	AC characteristics of IO port	●	●
	USART3 and FSMC remapping	●	●
System	PWR sleep mode	●	●
Clock	HSE serves as the clock source	●	●
	PLL frequency multiplication	●	●
USBD/CAN	Combined use of USBD/CAN	●	●
	CAN2_IO remapping	●	●
SPI	Module timing of SPI	●	●
Flash	Low-power wake-up	●	●
	Flash erase	●	●
Wake-up in Standby Mode	Operations before entering Standby mode	●	●

Note: "●" indicates that this errata description is involved in this version; the 'X' indicates that it is not involved in this version.

3 GPIO

3.1 GPIO output

Problem description

When the GPIO port is configured as multiplexing push-pull output, the output voltage may be affected by external interference and is unable to output accurate levels; when configured as floating input to read the external I/O input values, it may be affected by external interference and is unable to read accurate values.

Solutions

When configured as multiplexing push-pull output, connect an external pull-up resistor; when configured as floating input, connect an internal pull-up resistor externally or configure it as a pull-up input.

3.2 AC characteristics of IO port

Problem description

AC characteristics of GPIO_IO: PA8 and PC8 are equipped with an external 50pF load capacitor. At 2V low voltage, the output rate is 10MHz square wave, and the output duty cycle is high, ranging from 60% to 70%.

Solutions

It is recommended to avoid the simultaneous occurrence of low-voltage and low-speed (2V, 10MHz) conditions when this pin is used.

The I/O speed is related to the configuration, normal at high speed and abnormal at low speed. For example, if I/O is configured to 50MHz mode and outputs 10M at 2V, the duty cycle is normal.

3.3 USART3 and FSMC remapping

Problem description

USART_USART3 remapping PD8 and PD9 pins conflicts with FSMC clock. Specifically: when remapping PD8 and PD9 as serial pins, enable FSMC clock but the serial communication cannot be used normally.

Solutions

Choose either of the following solutions:

- Use partial remapping function or default configuration of USART3.
- When USART3_TX is remapped to PD8 as a serial port pin, disable the SMC function.

4 System

4.1 PWR sleep mode

Problem description

The PWR sleep mode_WEF() instruction is invalid and cannot enter the low-power mode.

Solutions

Choose either of the following solutions:

- It can be executed normally after it is reset through the reset pin.
- Set in the download of Keil (set the reset and run)
- Add the second WFE instruction and it can be executed normally.
- Modify the program, and use 1 WFI rather than WFE.

5 Clock

5.1 HSE serves as the clock source

Problem description

When the timeout value of the software that sets the HSE startup time is too small (e.g. 0x0500), external clock startup ready timeout may occur, which may result in the failure of using HSE as the clock source.

Solutions

To ensure normal startup of the crystal oscillator, it is recommended to modify the external clock wait time timeout value to at least 0x3200.

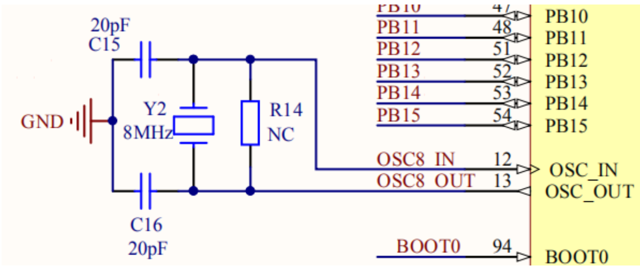
The specific operation is modifying the macro definition of HSE_STARTUP_TIMEOUT. Macro definition varies depending on the version of the library function:

- For the V3.x version library functions, the macro definition is in XXX32F10x.h;
- For the library before V3.0, the macro definition is in XXX32f10x_RCC.c.

The recommended crystal oscillator circuit is shown below (the capacitance value should match the crystal oscillator model)：

#define HSE_STARTUP_TIMEOUT ((uint16_t)0x3200) (recommended 0x3200, maximum 0xffff).

Figure 1 Crystal Oscillator Circuit



5.2 PLL frequency multiplication

Problem description

After doubling to 24MHz using PLL, the frequency output through the PA8 pin is unstable.

Solutions

When using PLL multiplication, first use a large multiplication coefficient to increase the frequency of the VCO, and then output at a lower frequency. For example, increase the PLL frequency to 48MHz and then divide its frequency to 24MHz through an AHB prescaler.

6 USBD/CAN

6.1 Combined use of USBD/CAN

Problem description

USBD1 and CAN2 of APM32F103xC can be used simultaneously, USBD2 and CAN1 can be used simultaneously, USBD1 and USBD2 cannot be used simultaneously, and CAN1 and CAN2 can be used simultaneously.

Solutions

Use according to the recommendations of *Datasheet* and *User Manual*.

6.2 CAN2_IO remapping

Problem description

When multiple groups of peripheral I/O remap the configuration, if CAN2 remaps the configuration first and then other peripherals remap the configuration, CAN2 will fail to remap.

Solutions

Put the CAN2 remapping operation behind the remapping operation of other peripherals.

7 SPI

7.1 Module timing of SPI

Problem description

When SPI (SPI_cmd() function ENABLE) is enabled, after SPI parameters are modified, the timing transmission of SPI for one byte is 16 clocks (normally 8 clocks).

Solutions

The initialization standard operation of SPI is specifically:

Initialize the corresponding SCK MOSI, MISO and NSS, and enable SPI. To modify the parameters, first enable SPI (SPI_cmd() function DISABLE) and then modify the corresponding configuration.

8 Flash

8.1 Low-power wake-up

Problem description

The low-power and AHB frequency division scenario may result in abnormal clearing of the dcode buffer, thus entering hardfault.

Solutions

For the WFI and WFE low-power wake-up scenarios:

- For the WFI low-power wake-up scenarios, AHB should not divide the frequency (i.e. ensure that the first interrupt vector data is read and returned from Flash, rather than returned from buf). After the low power is awakened, enter the interrupt service function, first read an address from each Flash bank in the interrupt service function and then start to execute the real user program.
- For the WFI low-power wake-up scenarios, AHB should not divide the frequency (i.e. ensure that the first interrupt vector data is read and returned from Flash, rather than returned from buf). After the low power is awakened, start sequential execution, first read an address from each bank and then start to execute the real user program.

8.2 Flash erase

Problem description

The erase operation and read Flash operation are performed concurrently, and a read Flash data error occurs when the erase operation is completed:

- The program executes FLASH->SR status register in sequence, and read errors may occur.
- In the process of erasing Flash, an interrupt occurs, and the interrupt service function contains a program of reading data from Flash, and data errors may occur when erasing is completed, and thus causes program exceptions.

Solutions

Choose either of the following solutions:

- For regular erase scenarios (program sequential execution), after initiating erase, before executing FlASH_GetBank1Status, add:
  while (FLASH->SR&FLASH_FLAG_BANK1_BSY)==FLASH_FLAG_BSY;
  And AHB keeps the frequency not divided.
- For regular erase scenarios (program sequential execution), after the state is read for the first time, it will be executed once again before the total state returns:
  FLASH_GetBank1Status sub-function
  And AHB keeps the frequency not divided.

- For the interrupt scenarios, before erasing Flash, shield the interrupt, there will be no scenarios of entering the interrupt in the erasing process, and it will change to the regular erase scenario.
- For the interrupt scenarios, add a statement of waiting for the Flash erase operation to end at the beginning of the interrupt service function:
  while (FLASH->SR&FLASH_FLAG_BANK1_BSY)==FLASH_FLAG_BSY;
  Wait for the Flash erase operation to end, then execute the interrupt service program, and keep the AHB frequency not divided.

9 Wake-up in Standby Mode

Problem description

In Standby mode, the system supports multiple wake-up sources. These signals are combined (using a logical OR) before reaching the rising edge detector. When a valid edge is detected, a wake-up flag (WUEFLG) is generated. To ensure the MCU enter and stay in Standby mode, you must clear the WUEFLG flag first; otherwise, it will wake up immediately. Note that if any active wake-up source stays high while clearing the flag (setting the WUFLGCLR bit), the detector's input also stays high. As a result, it cannot detect new level changes, which masks future wake-up events and prevents the MCU from waking up properly.

Solution 1

To prevent this issue, follow these steps before entering Standby mode:

(1) Disable all used wake-up sources.

(2) Clear all related wake-up flags.

(3) Reenable all used wake-up sources.

Solution 2

Keep only one wake-up source before entering Standby mode (for example, turn off the RTC alarm and leave only the PA0 WKUP function on).

10 Revision history

Table2 Document Revision History

Date	Version	Revision History
August 2024	1.0	● Initial release
April 2026	2.1	● Delete Chapter 2: Product Version and Silk Screen Printing Instructions ● Add Chapter 9: Wake-up in Standby Mode

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